338

	Chuan-Hu	rate single-phase clocking of a closed pipeline including wave pipelining, stoppability, and startability is Chang, Davidson, E.S., Sakallah, K.A.,	
		-Added Design of Integrated Circuits and Systems, IEEE Transactions on 4. Issue 12, Dec. 1995 Page(s):1526 - 1545	
		ect Identifier 10.1109/43 476583	
			AbstractPlus Full Text. PDF(1820 KB) IRRE PAS. Rights and Permissions
	2	A Single-Stream Pipelined Instruction Decompression System for Embedded Microprocessors Yuan-Long Jeang, Tzuu-Shaang Wey, Hung-Yu Wang, Chih-Chung Tai,	
		Intelligent Information Hiding and Multimedia Signal Proceeding, 2006. IHH-MSP '06. International Conference on Dec. 2006 Page(s):571 - 574 Digital Object Identifier 10.1109/IH-MSP 2006 265067	
		AbstractRus Full Text PDE(196 KB) IEEE CNF Rights and Fermissions	
П	3.	A New and Efficient Field-Partition Based Code Compression and its Pipelined Decompression System Yuan-Long Jeang; Chih-Chung Tai; Yong-Zong Lin; Incovates Compating, Information and Control, 2028. ISCIQ V6. First International Control Code.	
		Volume 2, 30-01 Aug. 2006 Page(s):10 - 13 Digital Object Identifier 10 1109/ICICIC 2006 206	
		AbstractPlus Full Text: PDE(152 KB) :EEE CAF	
		Rights and Permissions	
	4.	Interfacing synchronous and asynchronous modules within a high-speed pipeline Spagen. A.E. Myers, C.J.; Synchronous Synchronous Synchronous IEEE Transactions on Volume 8, 1899, 5, Oct. 2000 Page(s):573 - 583 Digital Cheir Cheffer 10 1109/82 994 162	
		Abstractifius Befetenas Full Text: PDE(176 KB) IEEE INL. Flighte and Permissions	
	5.	An Efficient Field-Partition Based Code Compression and its Pipelined Decompression System Yuan-Long Jeang: Yong-Zong Lin, VLSI-Spasin, Automation and Test 2009 International Symposium on April 2009 Fage(e): 1 - 4 Digital Chyeric Martin Fer to 1104/VDAT 2006 258133	
		AbstractPlus Full Text: PDE(8666 KB) HEES CNF Rights and Permissions	
	6	Interfacing synchronous and asynchronous modules within a high-speed pipeline Spgren, A.E., Myers, C.J., Advanced Besearch in V.L.S., 1997, Proceedings, Seventeenth Conference on 15-16 Sept, 1997, 2page (147-61).	
		Digital Object Identifier 10 1109/ARVLSI 1997 634845	
		AbstractPlus Full Text: PDE(808 KB) IEEE Chif Rights and Permissions	
	7.	Exploiting Low Entropy to Reduce Wire Delay Otron. D.; Computer Architecture Lotters Volume 3, Issue 1. Jan. 2004 Page(s): 1 - 1 Digital Cheir Latterfier 10 110(s): C.2004 7	
		Abstractiblus Full Text: PCIE(200 KB) SEEE INC. Rights and Permissions	

	8.	Workload characterization for the design of future servers Mance, B., Chen, T., Vianney, D., Ciswak, B., Kurikel, S., Mericas, A.; Workload Characterization Symposium, 2005. Proceedings of the JEEE International 6-8 Cut, 2006 Page(e); 129 - 138 Digital Object Identifier 10.1 109/ISWC 2005.1526009 Abdzpac(Flux) Full Text: PCE(423 KB) 6EEE CUF
		Blights and Permissions
O	9.	Context-aware task assignment in ubiquitous computing environment - A genedic algorithm based approach Pawar, Pawar, Me, Isalang, Woya, Ing, van Belpium, Ben-Jain, van Isalaren, Aart; Evidancing/Considiaties, PAZIL, CEZ, GEZO, JEEE Conguess on 28-28 Sept. 2007 Page(s) 2005 2-2702 Digital Object Identific 10.1106/CEC 2007-4424611
		AbstractPlus Full Text, PDF(309 KB) IE FE CNF Rights and Permissions
	10	A deterministic globally asynchronous locally synchronous microprocessor architecture Heath, M., Harris, I.
		Microprocessor Test and Verification: Common Challenges and Solutions, 2003. Proceedings, 4th International Workshop on
		29-30 May 2003 Page(s):119 - 124
		AbstractPlus Full Text: POF (265 KB) 16 SE CNF
		Slatte and Dominicians